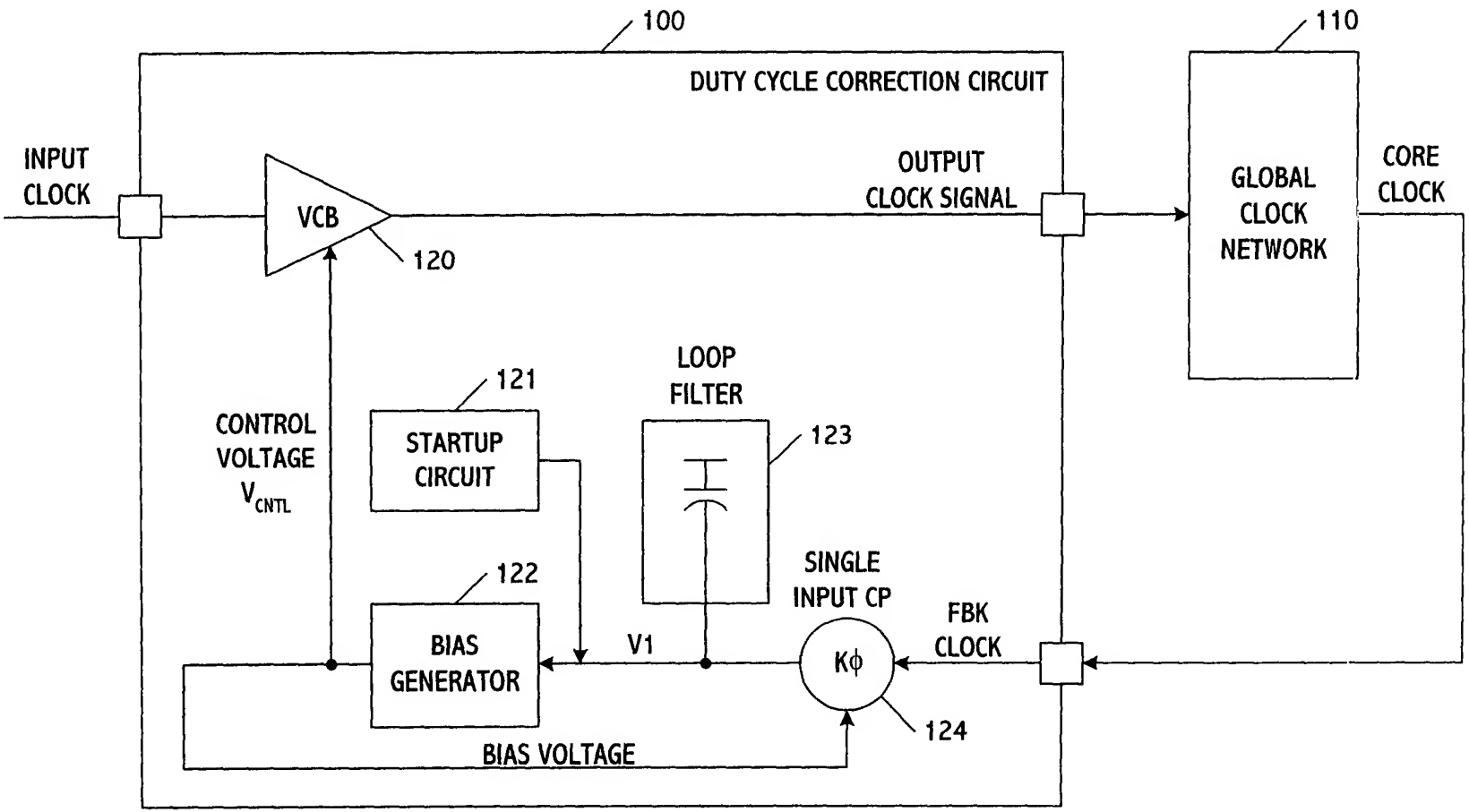

100
DUTY CYCLE CORRECTION CIRCUIT
110
INPUT CLOCK
VCB
120
OUTPUT CLOCK SIGNAL
GLOBAL CLOCK NETWORK
CORE CLOCK
LOOP FILTER
121
CONTROL VOLTAGE V_{CNTL}
STARTUP CIRCUIT
123
SINGLE INPUT CP
122
FBK CLOCK
BIAS GENERATOR
V1
Kϕ
124
BIAS VOLTAGE

FIG. 1

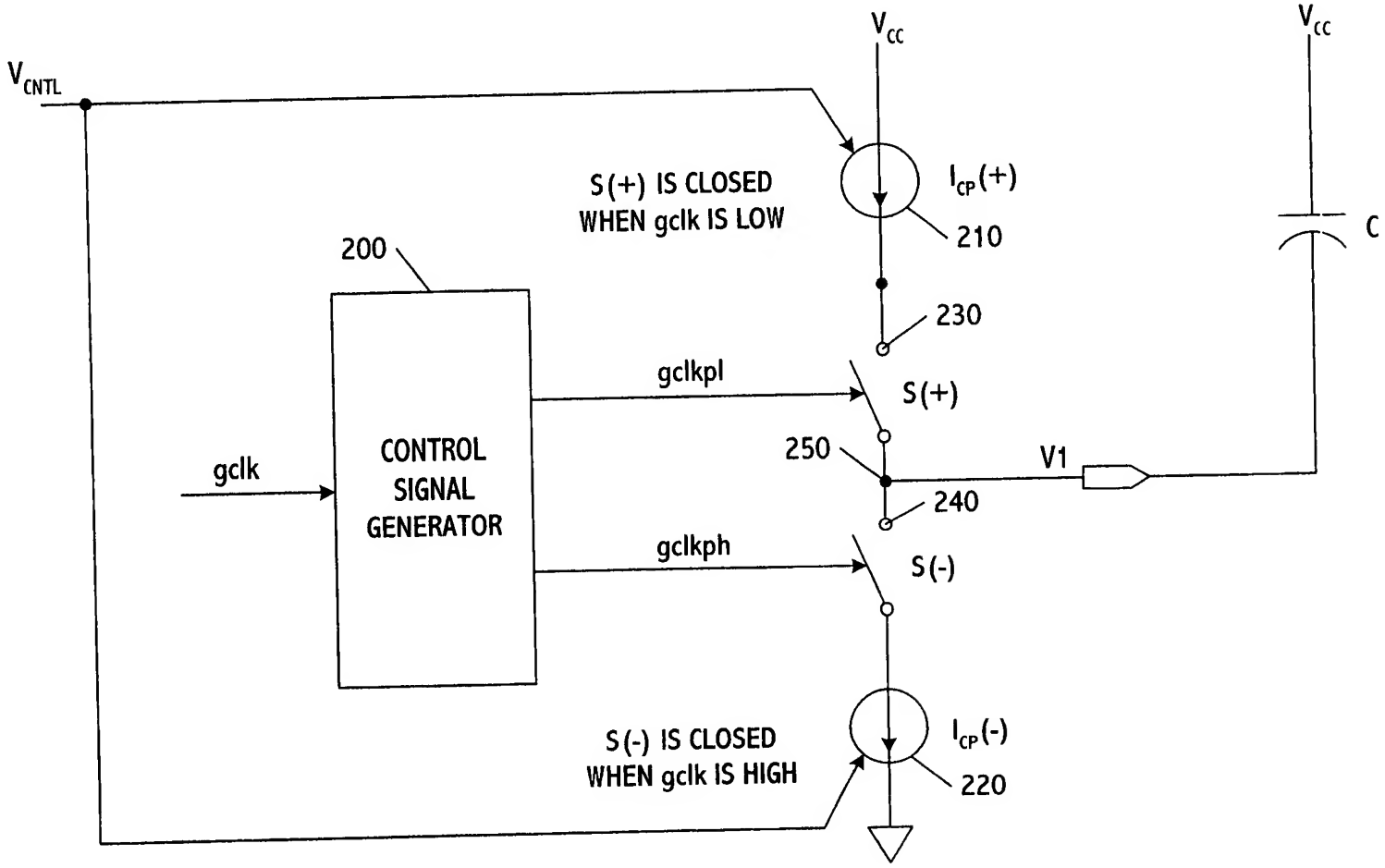

V_{CNTL}
V_{CC}
V_{CC}
S(+) IS CLOSED
WHEN gclk IS LOW
$I_{CP}(+)$
210
C
200
230
gclkpl
S(+)
gclk
CONTROL
SIGNAL
GENERATOR
250
V1
240
gclkph
S(-)
S(-) IS CLOSED
WHEN gclk IS HIGH
$I_{CP}(-)$
220

FIG. 2

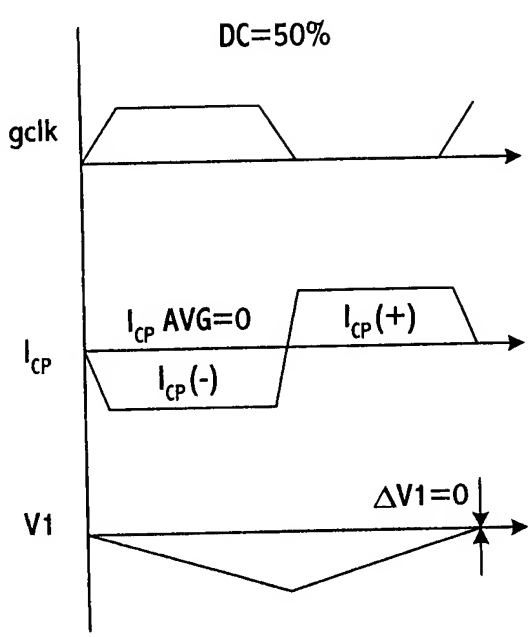


FIG. 3(a)

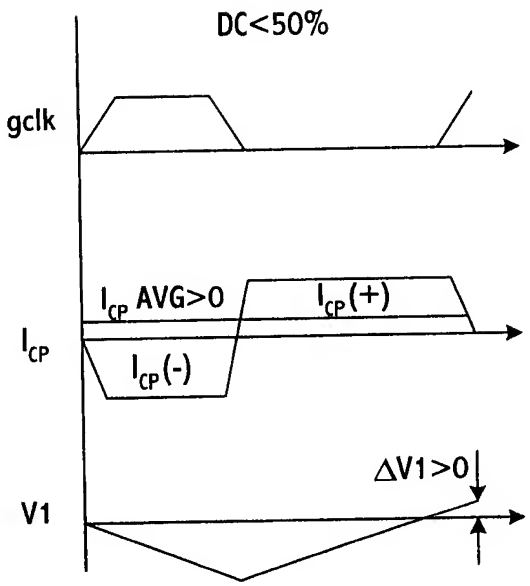


FIG. 3(b)

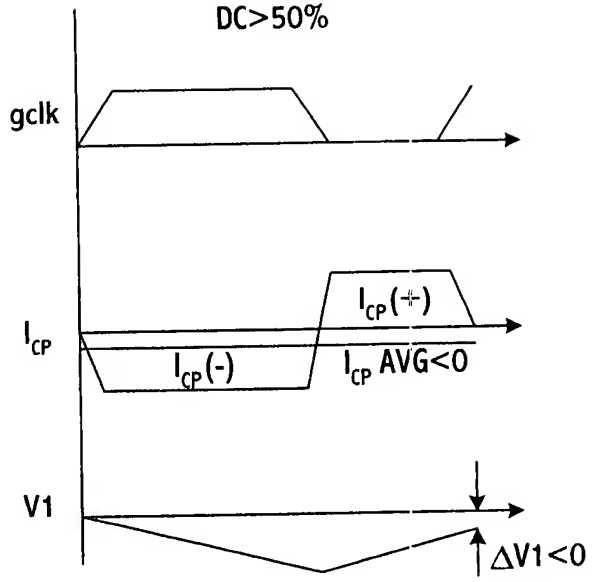


FIG. 3(c)

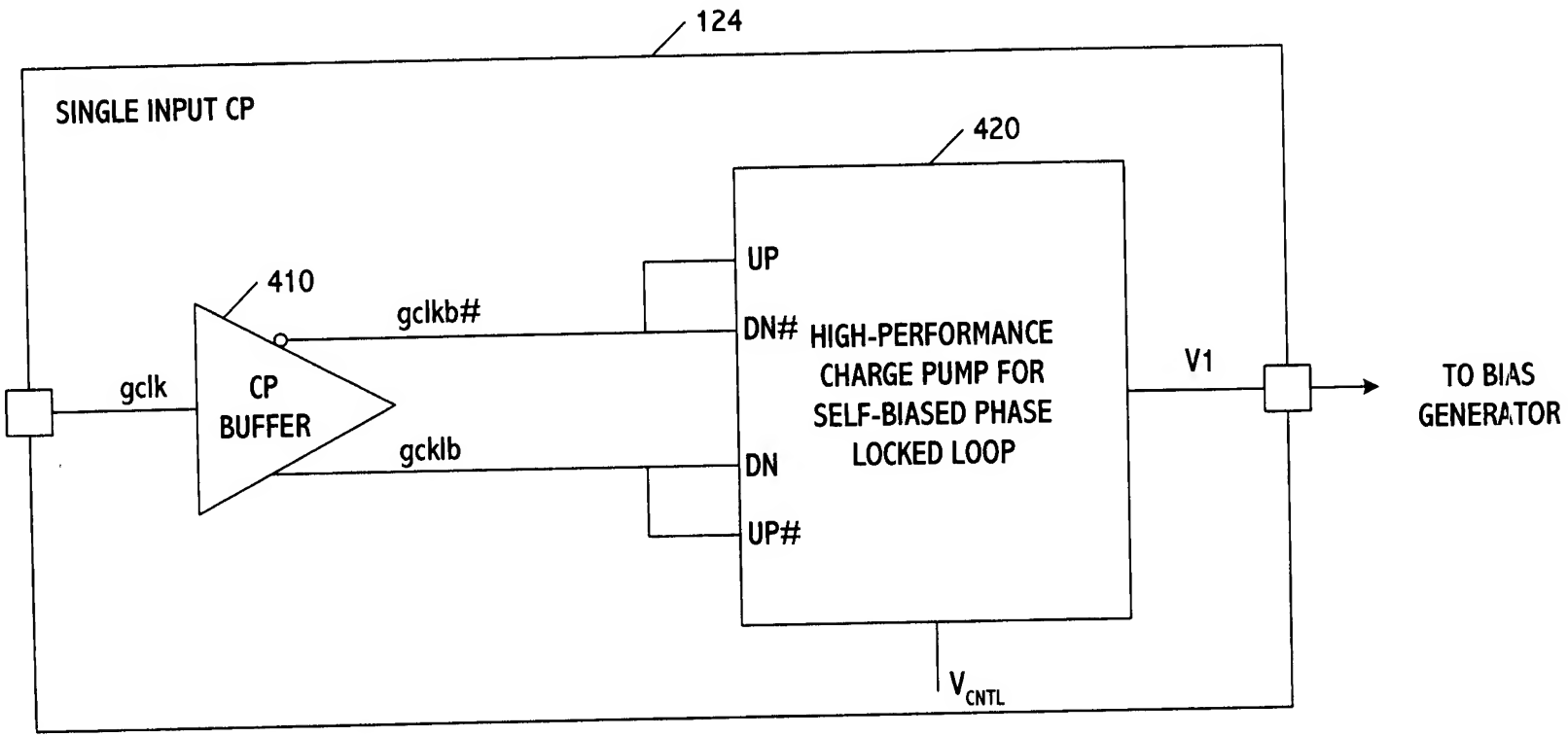

124
SINGLE INPUT CP
420
410
UP
gclkb#
DN#
HIGH-PERFORMANCE
CHARGE PUMP FOR
SELF-BIASED PHASE
LOCKED LOOP
V1
TO BIAS
GENERATOR
gclk
CP
BUFFER
gcklb
DN
UP#
V_{CNTL}

FIG. 4

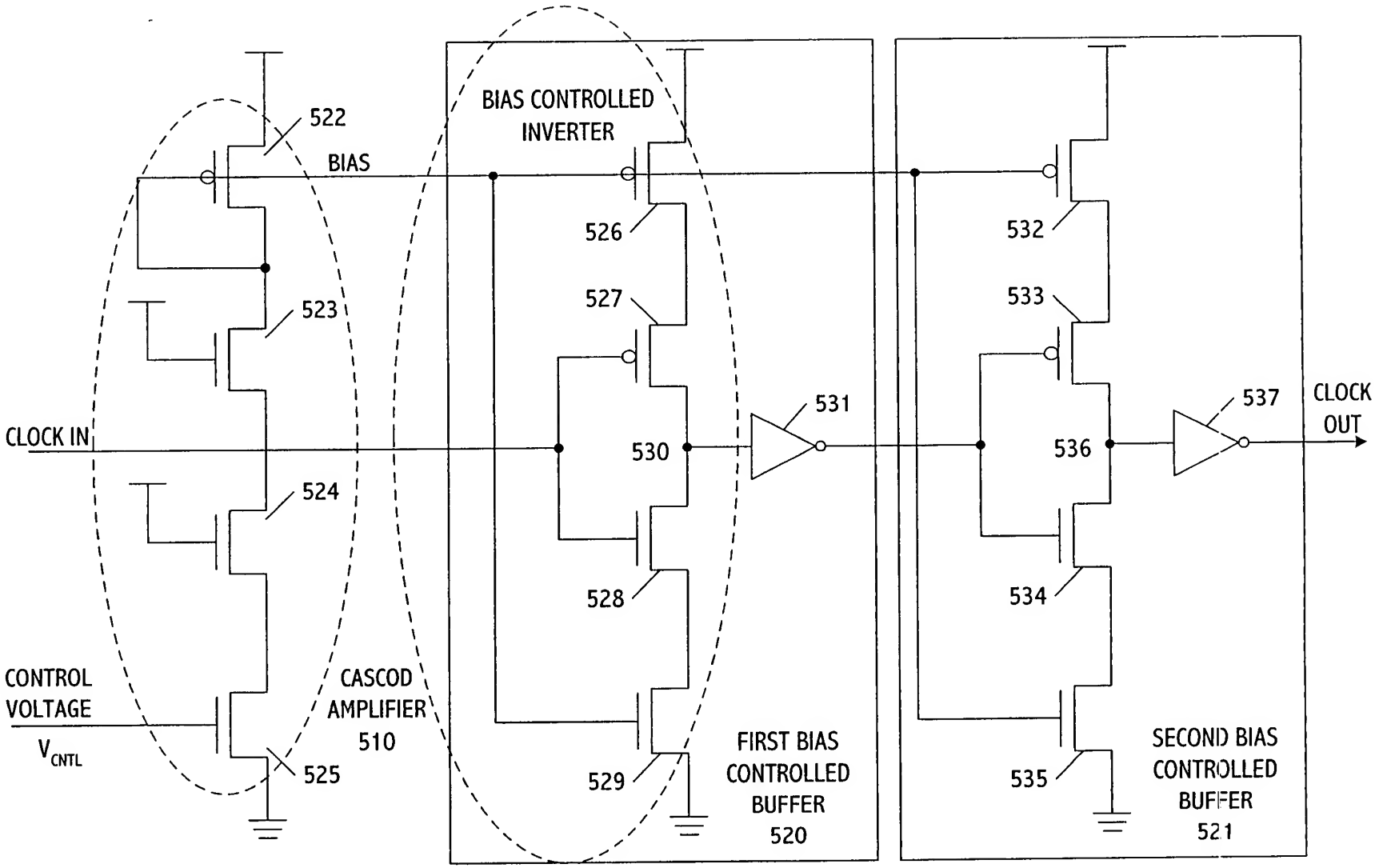
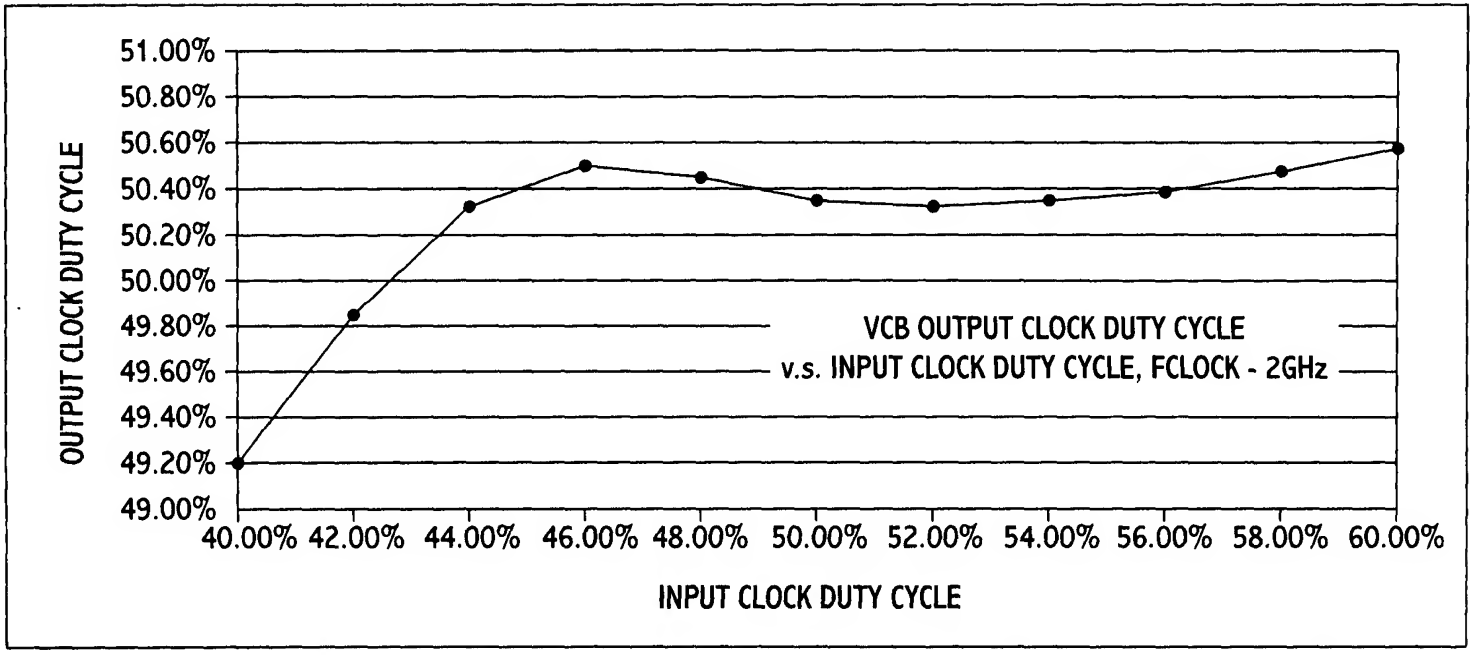
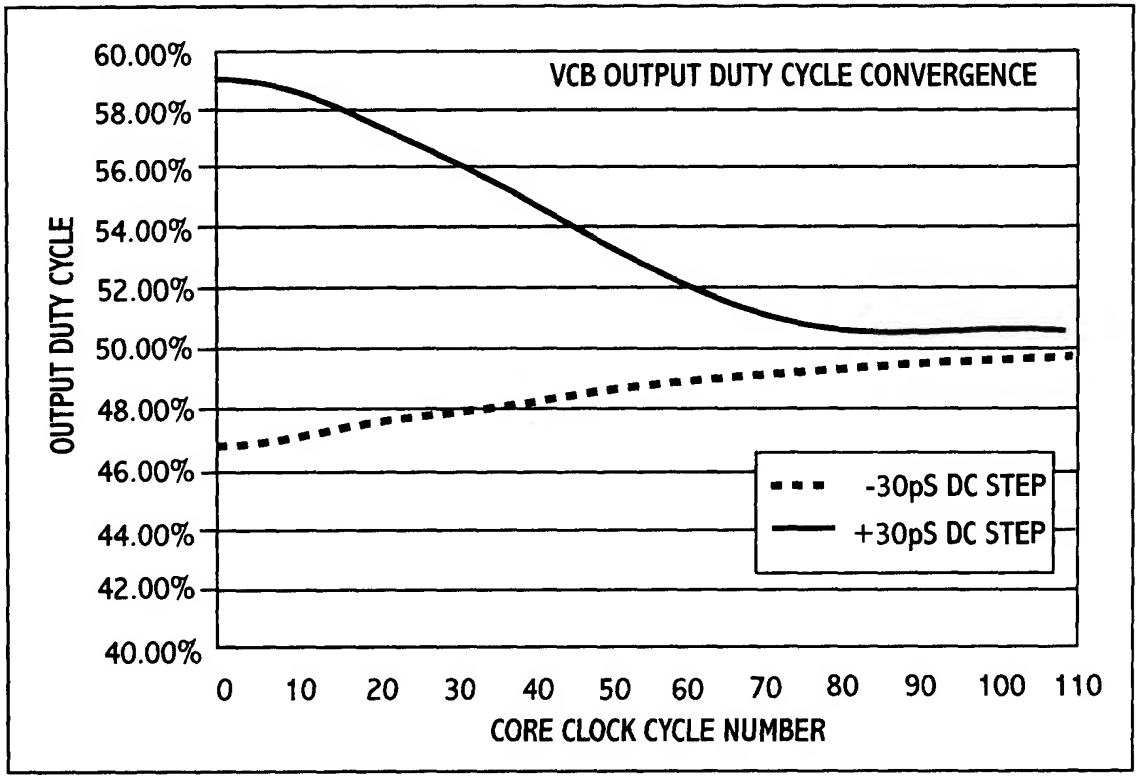

BIAS CONTROLLED
INVERTER
522
BIAS
526
532
523
527
533
CLOCK IN
531
537
CLOCK
OUT
530
536
524
528
534
CONTROL
VOLTAGE
V_{CNTL}
CASCOD
AMPLIFIER
510
525
529
535
FIRST BIAS
CONTROLLED
BUFFER
520
SECOND BIAS
CONTROLLED
BUFFER
521

FIG. 5



DUTY CYCLE CORRECTION CIRCUIT PERFORMANCE

FIG. 6



DUTY CYCLE CIRCUIT CONVERGENCE

FIG. 7

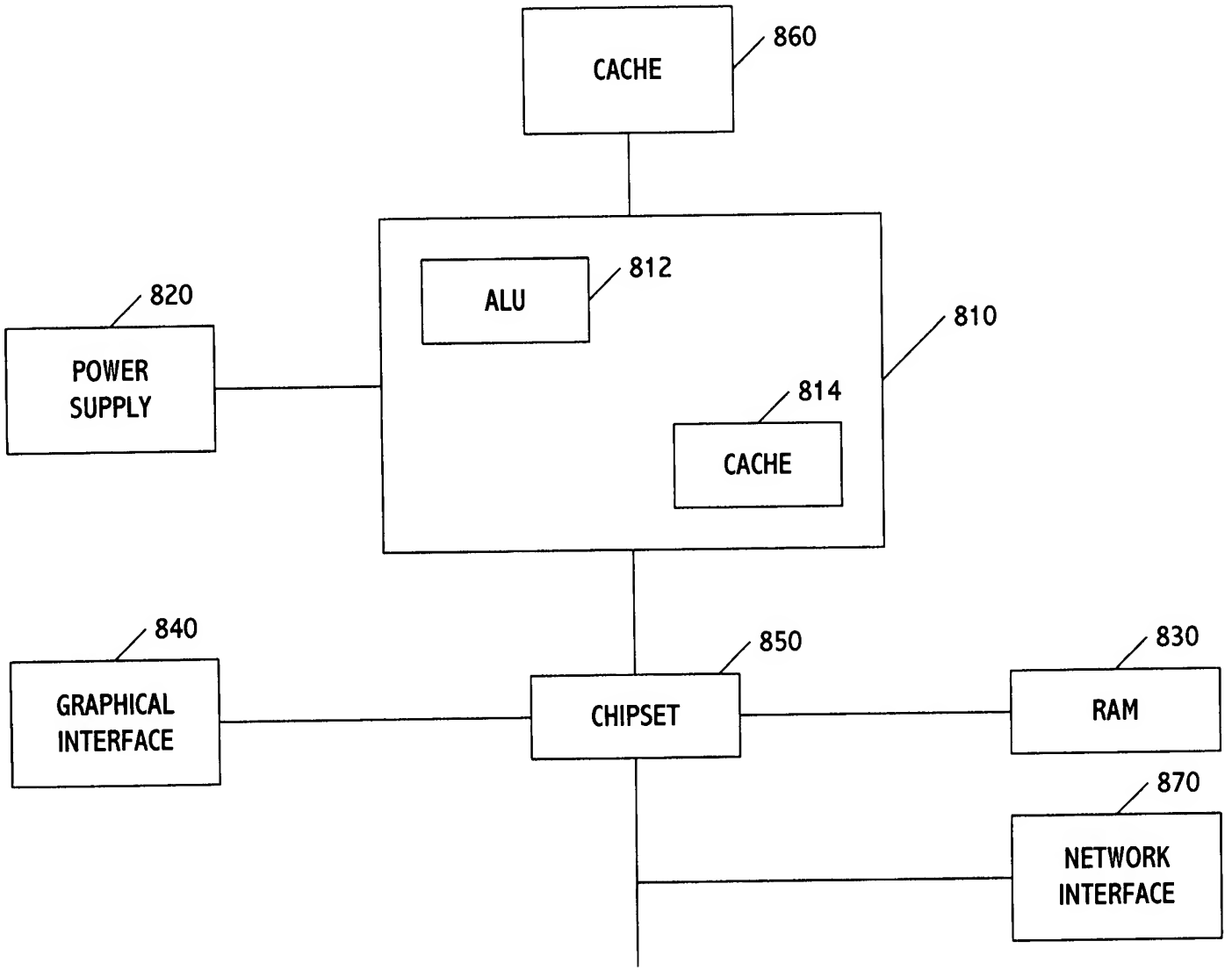

CACHE
860
ALU
812
810
820
POWER SUPPLY
814
CACHE
840
GRAPHICAL INTERFACE
850
CHIPSET
830
RAM
870
NETWORK INTERFACE

FIG. 8